

APPLICATION
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TITLE: METHOD FOR FORMING FERROCAPACITORS AND
FERAM DEVICES

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Method for forming ferrocapacitors and FeRAM devices

Field of the invention

The present invention relates to methods for forming ferrocapacitors of the kind used in FeRAM devices, and to methods for forming FeRAM devices themselves. The invention further relates to FeRAM devices including
5 ferrocapacitors formed by the method.

Background of Invention

Many conventional FeRAM devices include a horizontal ferrocapacitor
10 structure, in which a stack of layers is formed including top and bottom electrodes sandwiching a ferroelectric layer. An alternative "vertical capacitor" structure was suggested in US 6,300,652, the disclosure of which is incorporated herein by reference. A vertical capacitor includes a ferroelectric element sandwiched between electrodes to either side, all at substantially the
15 same level in the FeRAM device.

The process steps of a conventional technique for forming a vertical capacitor structure are illustrated in Figs. 1 to 5. The vertical capacitors are typically formed over a substructure, which may for example be of the form shown in
20 Fig. 1 in which various electronic components 1 are connected to conductive plugs 3 which extend upwards through a matrix 5 (e.g. of TEOS (tetraethylorthosilicate)). The upper ends of the plugs 3 terminate in TiN/Ir barrier elements 7, having a top surface flush with the surface of the matrix 5.

25 As shown in Fig. 2, an insulating layer 9 of Al_2O_3 is formed over the surface of the matrix 5, and a layer of ferroelectric material 11 such as PZT (PbZrTiO_3) is formed over that.

As shown in Fig. 3, hardmask elements 13 are deposited in selected areas of the PZT layer 11, and the portions of the PZT and Al_2O_3 which are not protected by the hardmask elements 13 are etched all the way through, forming openings 17. During this process Al_2O_3 fences 15 are often formed on the sides of the remaining PZT.

The openings 17 are then filled with conductive material 19 such as IrO_2 , by depositing IrO_2 over the entire structure, as shown in Fig. 4, and chemical-mechanical planarization (CMP) polishing is performed to form a flat upper surface 21 which is partly the PZT 11 and partly the conductive material 19. Then, as shown in Fig. 5, an Al_2O_3 layer 23 is formed over the surface 21. The elements 19 of IrO_2 constitute electrodes, while the remaining PZT 11 forms the dielectric.

The vertical capacitor structure has great potential for reducing the cell size, especially if the etching taper angle of the remaining PZT 11 (i.e. the angle between the horizontal direction and the sides of the remaining PZT) is high. However, if the taper angle becomes close to 90° , the Al_2O_3 fences 15 are more likely to be formed. These fences 15 are difficult to remove (e.g. by a wet cleaning process), and dramatically reduce the Q_{SW} (i.e. the maximum charge which can be stored in the ferrocapacitor) because the insulating fences 15 reduce the effective area of the capacitor.

Summary of the Invention

The present invention aims to alleviate the above problem, at least partially, and in particular to provide a new and useful method for forming ferrocapacitors and FeRAM devices with improved properties.

In general terms, the present invention proposes that the etching of the ferroelectric material and Al_2O_3 layer is performed in a two stage process: in a

first stage only the ferroelectric material is etched to form openings in it, leaving the Al_2O_3 layer substantially intact (so that fences are not produced); then an electrode layer is deposited into the openings formed in the ferroelectric layer; then further etching is performed to form openings in the
5 Al_2O_3 layer. Thus, by the time the second etching step is performed, there are already electrodes overlying the sides of the ferroelectric material, without insulating fences in between.

Specifically, in a first aspect the invention proposes a method for forming a ferrocapacitor which include the steps of:

10 depositing a ferroelectric material over an Insulating layer;

 a first etching step of etching of the ferroelectric material to form openings in it,

 depositing an electrode layer into the openings formed in the ferroelectric layer;

15 a second etching step, after depositing the electrode layer, of etching the insulating layer at the bottom of the openings to form gaps in it; and

 inserting conductive material into the gaps.

The invention further provides the ferrocapacitor devices produced by the method, and FeRAM devices including such ferrocapacitors.

20 **Brief Description of The Figures**

Preferred features of the invention will now be described, for the sake of illustration only, with reference to the following figures in which:

 Figs. 1 to 5 show the steps of a convention method of forming vertical capacitors; and

Figs. 6 to 9 show the steps of a method which is an embodiment of the invention.

Detailed Description of the embodiments

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The method which is an embodiment of the invention will be explained with reference to Figs. 6 to 9. The vertical capacitor structure is formed in these figures over a substructure as shown in Fig. 1. Elements shown in Figs. 1 to 5 which exactly correspond to elements in Figs. 6 to 9 are illustrated by the same reference numerals.

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The first step of the method, as in the conventional method is for a layer 31 of an insulating material such as Al_2O_3 to be formed over the substructure, and for a thicker layer 33 of ferroelectric material (typically PZT) to be formed over the Al_2O_3 layer 31. Hardmask elements 34 are formed over the PZT layer 33 in a formation which exposes areas of the PZT (e.g. circular, square or rectangular areas) which overlie the barrier elements 7. Then, etching is carried out, using the hardmask elements 34 to form a plurality of openings 35 in the PZT, as shown in Fig. 6. However, in contrast to Fig. 3, the openings 35 do not extend through the whole of the PZT layer 33. Typically, a thin layer 37 of PZT remains at the bottom of the openings 35, and in particular the Al_2O_3 layer 31 is not disturbed.

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As shown in Fig. 7, a layer 39 of a conductive material, e.g. IrO_2 is then formed over the structure of Fig. 6, including in particular portions 41 on the sides of the openings. The portions 41 will constitute electrode elements in the completed ferrocapacitor device, as explained below. A possible thickness range for the layer 39 would be 15nm to 20nm.

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As shown in Fig. 8, further etching is performed. This further etching thins the layer 39 of conductive material in all places, and in particular removes completely the portions of the layer 39 at the bottom of the openings 35. Furthermore, the thin layer 37 of PZT at the bottom of the openings 35 is removed, and the openings 35 are extended through the Al_2O_3 layer 31, to form gaps in it at which the tops of the barrier elements 7 are exposed. During this process, it is possible that fences of Al_2O_3 will be formed on the portions 41 of the layer 39 on the sides of the openings, but nevertheless the entire sides of the remaining parts of the PZT layer 33 are in contact with the electrode elements 41, and therefore have no influence on the Q_{sw}

Subsequently, the openings 35 are filled with further conductive material 43, such as more IrO_2 . Then, as in the conventional method, CMP polishing is performed to form a flat upper surface 45 which is partly the PZT 33 and partly the conductive material 43. Then, an Al_2O_3 layer 47 is formed over the surface 45, to form the completed structure shown in Fig. 9. The conductive material 43 makes electrical contact with the barrier elements 7 and the electrode elements 41 remaining from the layer 39, thereby electrically connecting the electrode elements 41 with desired electrical components of the substructure.

Although only a single embodiment of the invention has been described in detail, many variations of the method are possible within the scope of the invention as will be clear to a skilled reader.